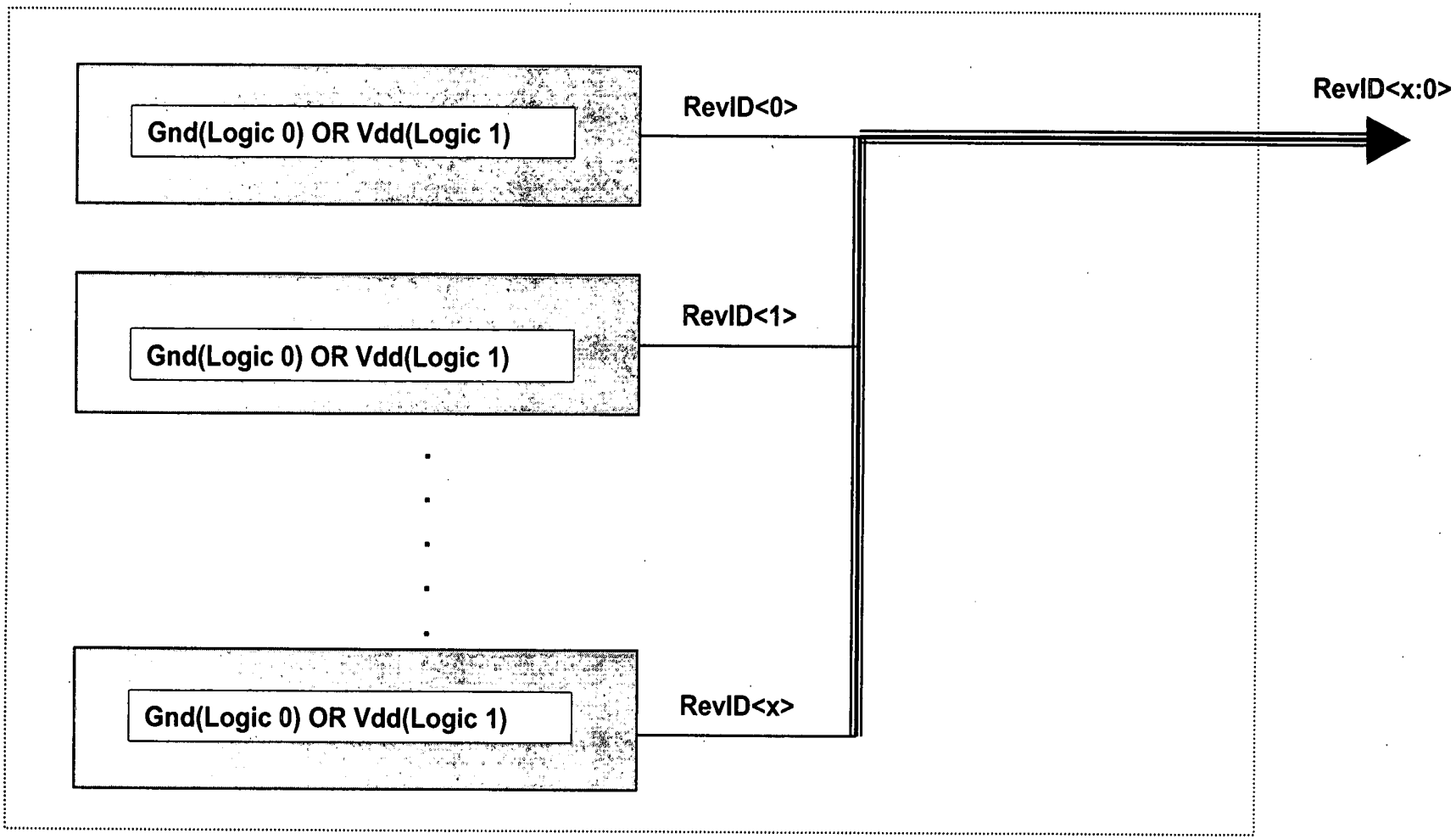

Gnd(Logic 0) OR Vdd(Logic 1)
RevID<0>
RevID<x:0>
Gnd(Logic 0) OR Vdd(Logic 1)
RevID<1>
Gnd(Logic 0) OR Vdd(Logic 1)
RevID<x>

FIG. 1

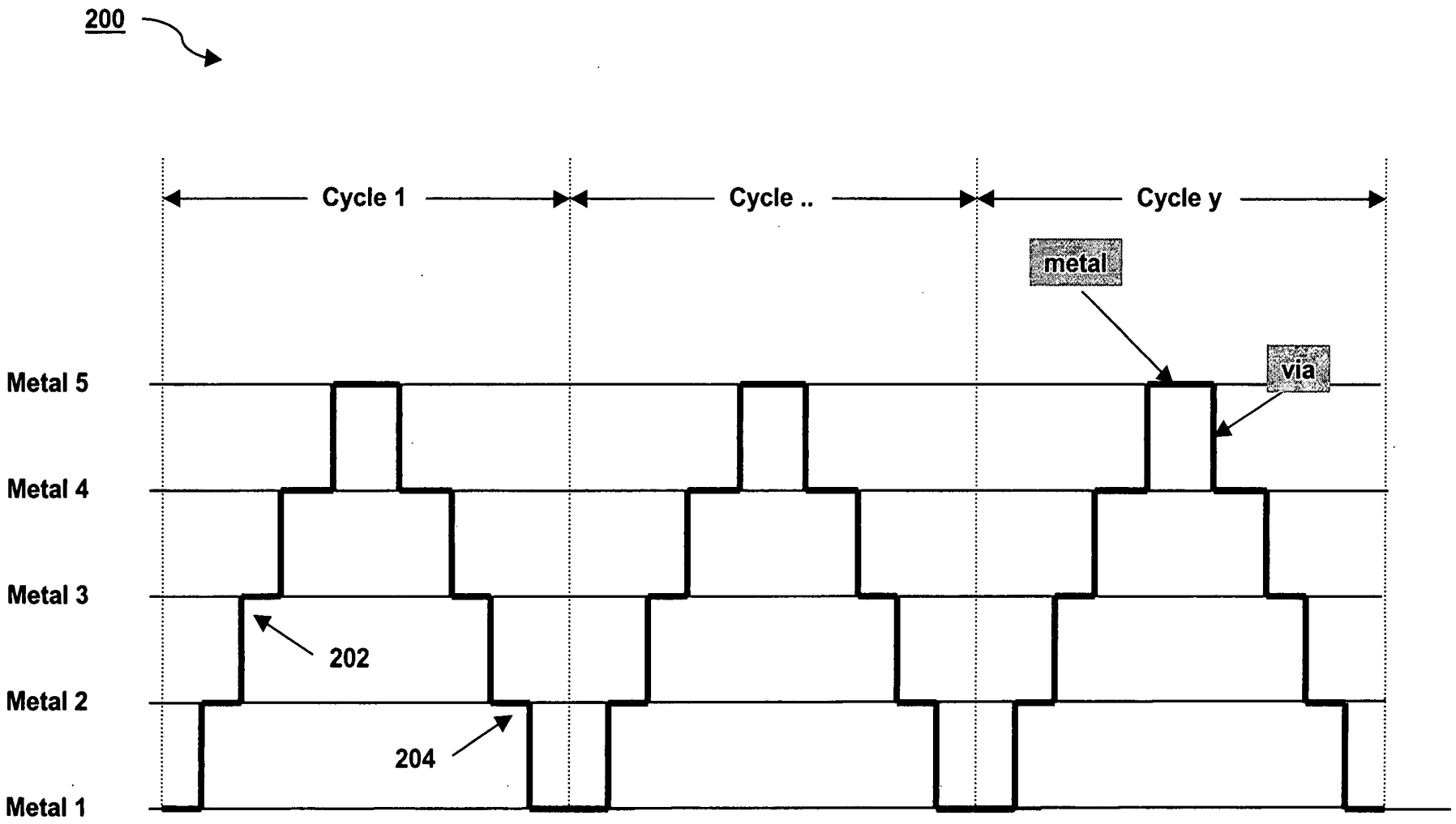

200
Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
202
204

FIG. 2

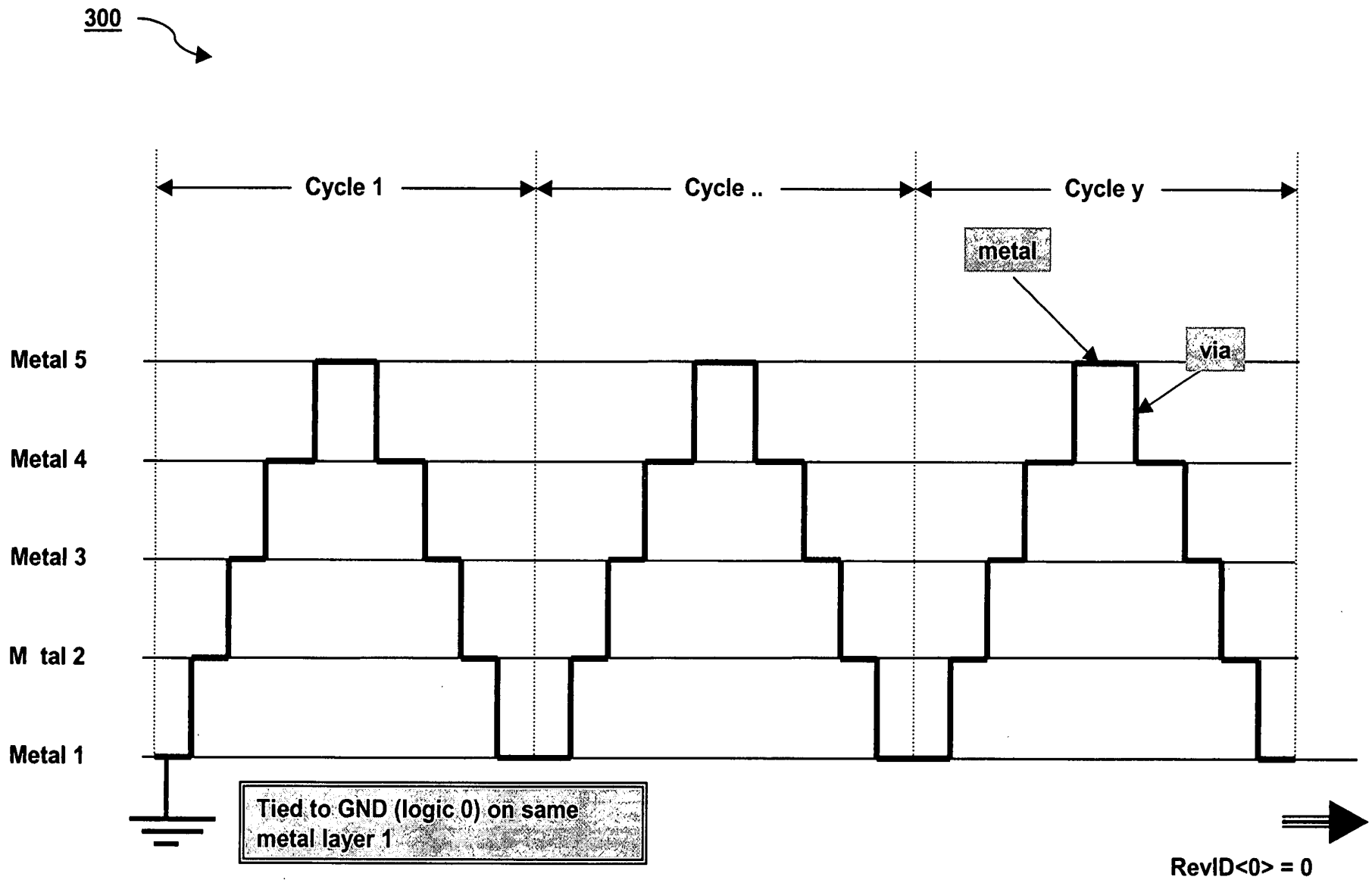

300
Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
Metal 3
M tal 2
Metal 1
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 0

FIG. 3A

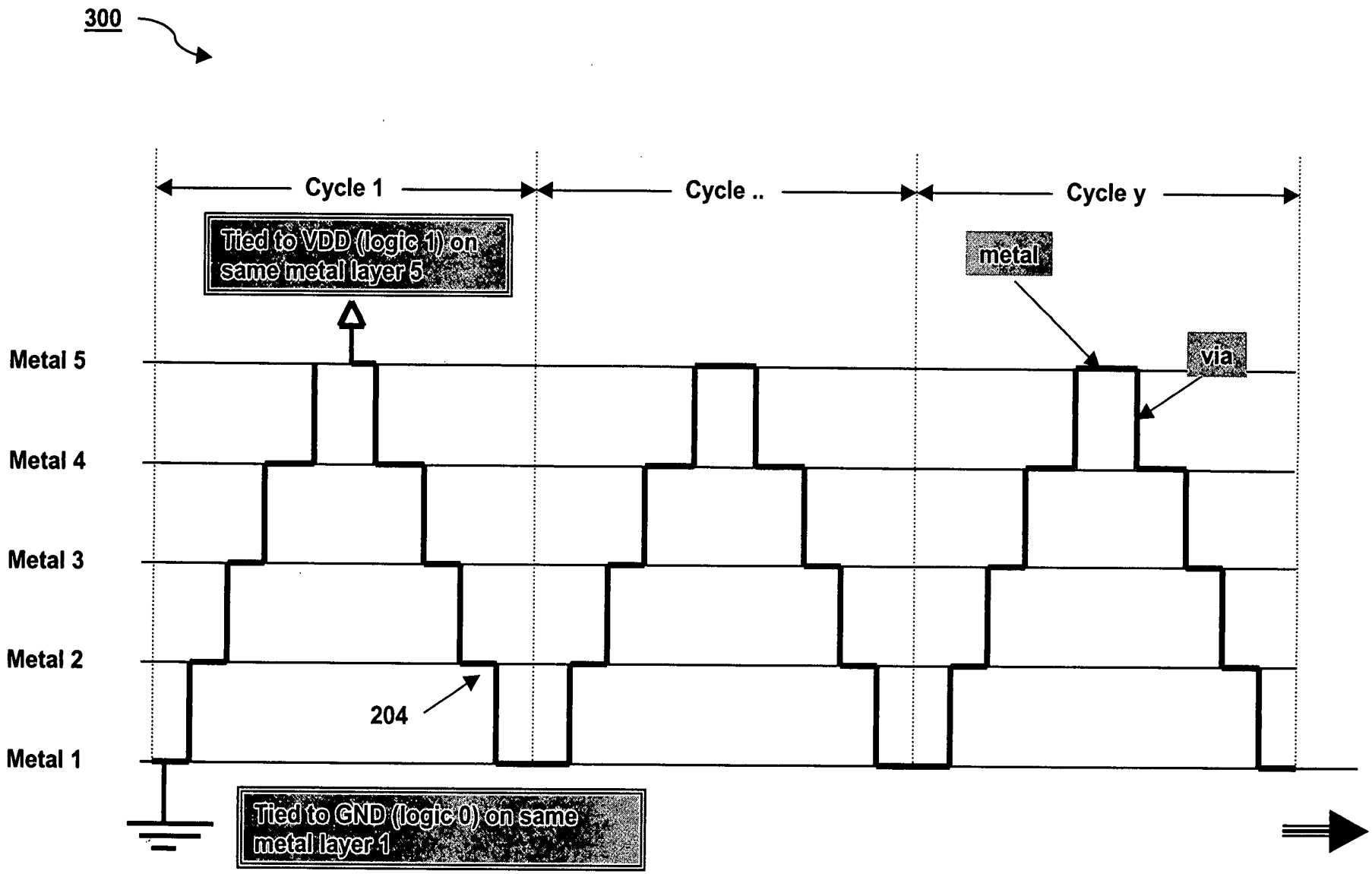

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
204
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 1

FIG. 3B

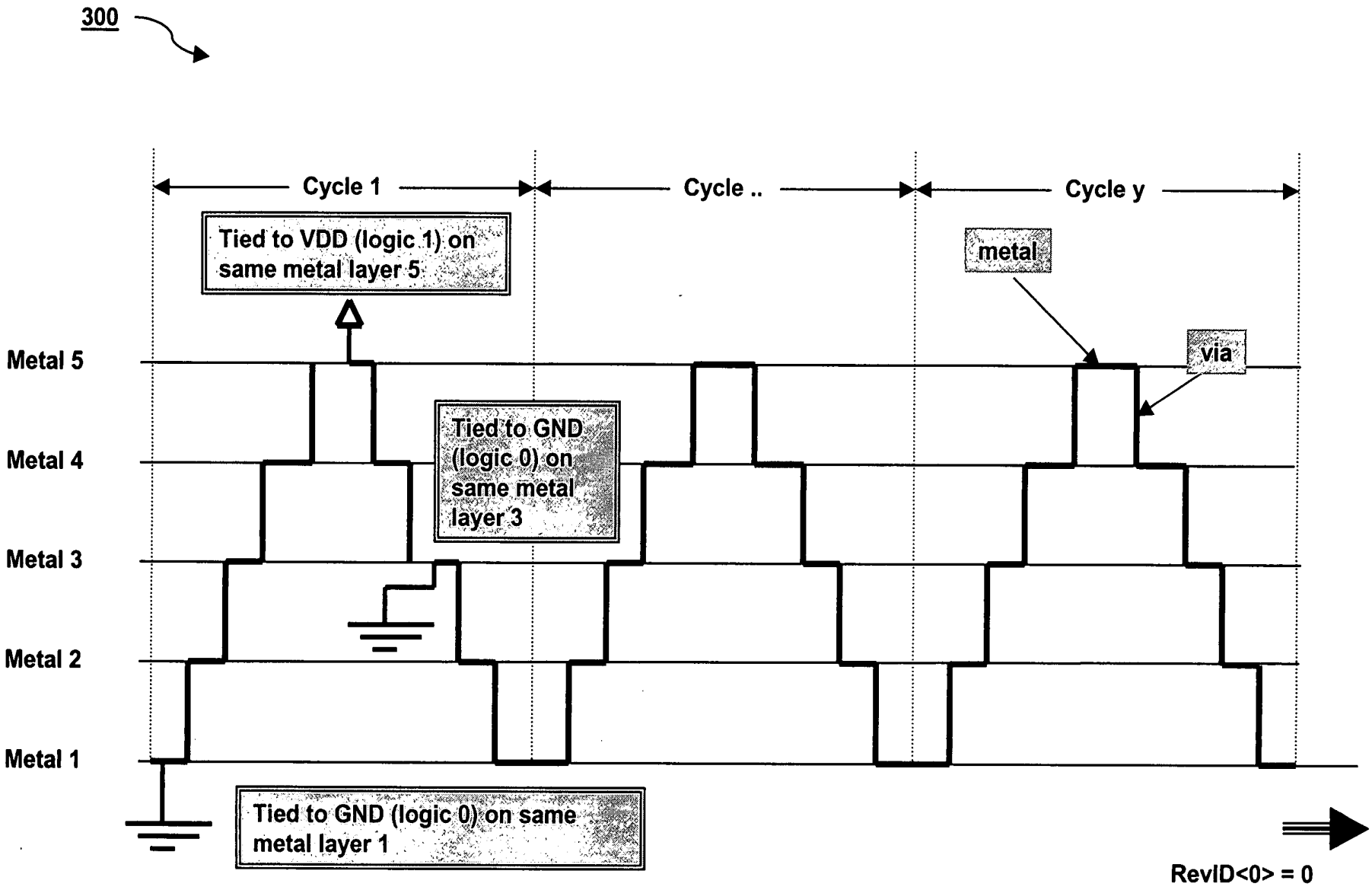

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Tied to GND (logic 0) on same metal layer 3
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 0

FIG. 3C

400

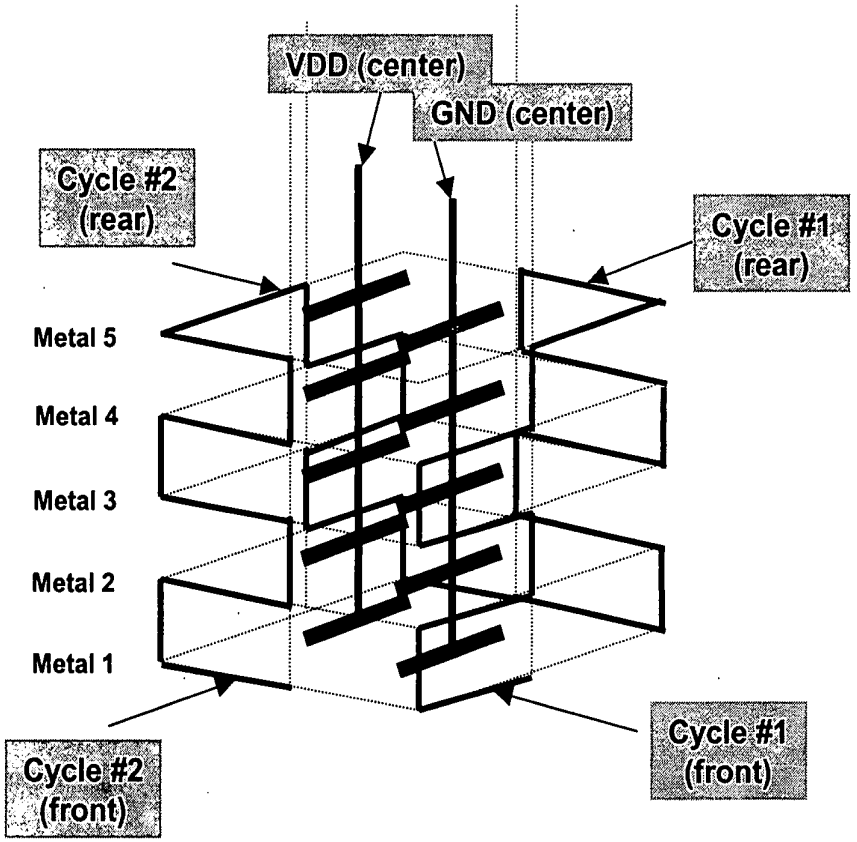

VDD (center)
GND (center)
Cycle #2 (rear)
Cycle #1 (rear)
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Cycle #2 (front)
Cycle #1 (front)

FIG. 4

500
GND (outside) available at all metal layers
Cycle #1 (outer spiral)
Cycle #1 (inner spiral)
VDD (outside) available at all metal layers
Cycle #2 (outer spiral)
Cycle #2 (inner spiral)
Metal 5
M tal 4
Metal 3
Metal 2
Metal 1
inter-cell connect
(502)

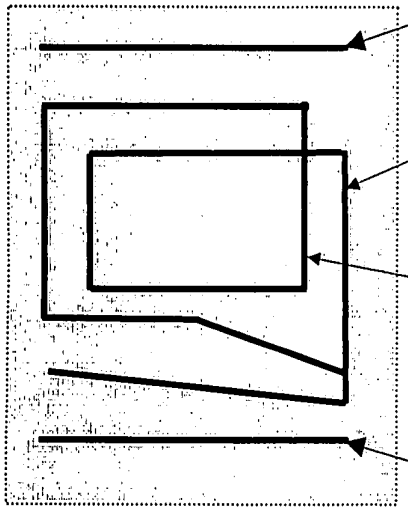


FIG. 5B

FIG. 5A

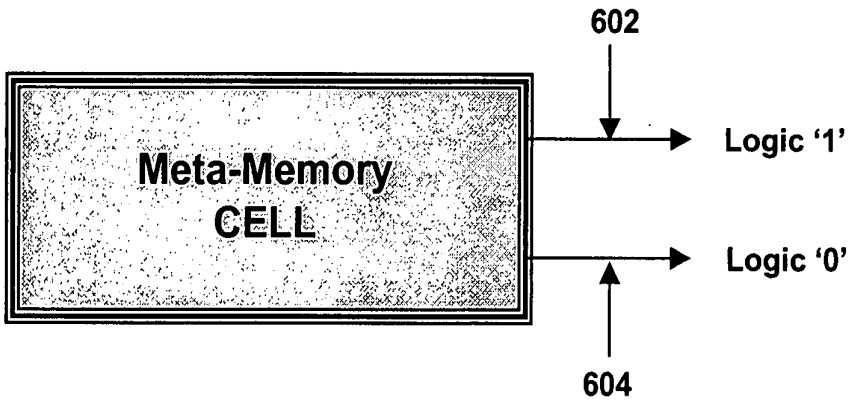


FIG. 6

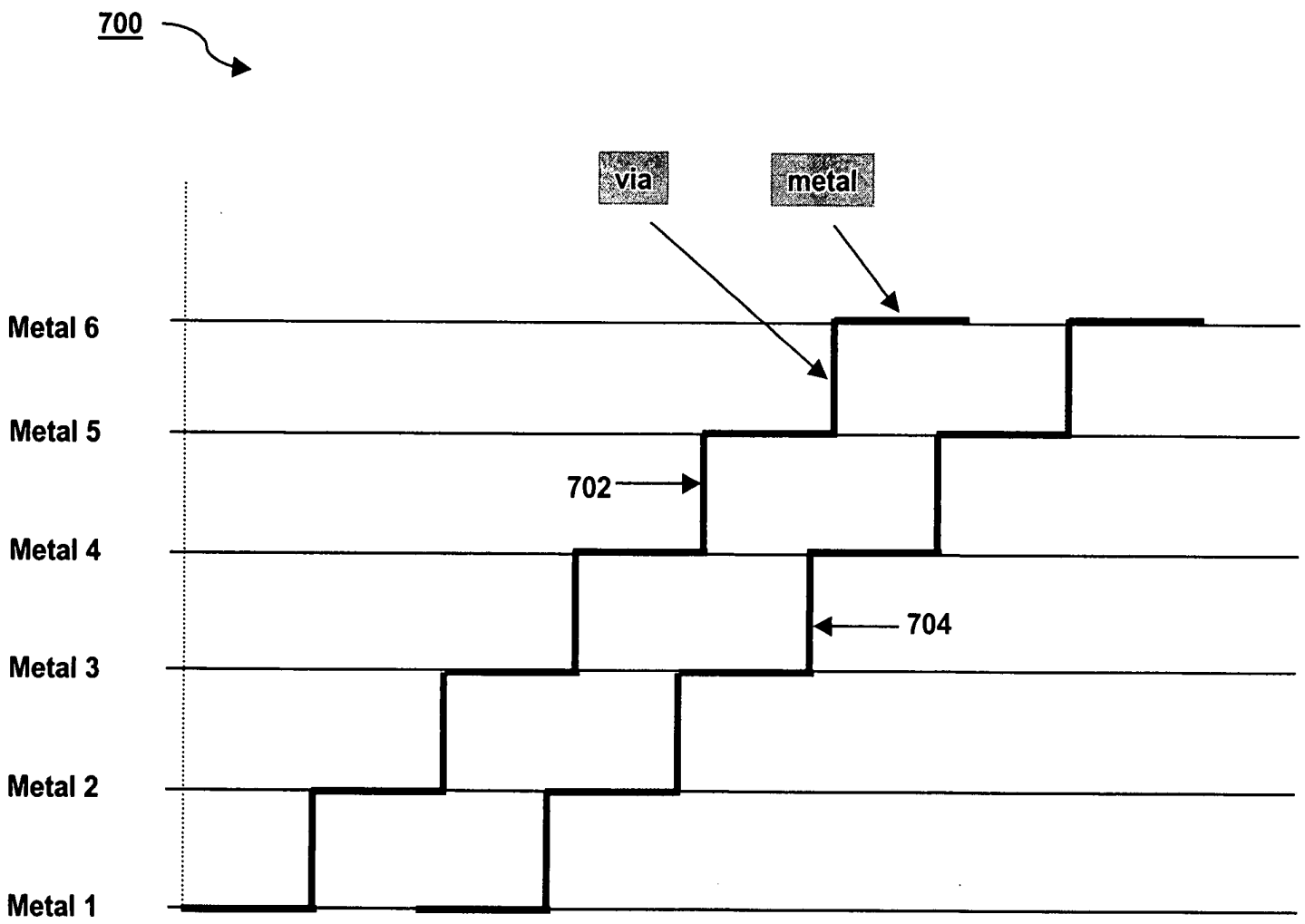

700
via
metal
Metal 6
Metal 5
702
Metal 4
704
Metal 3
Metal 2
Metal 1

FIG. 7A

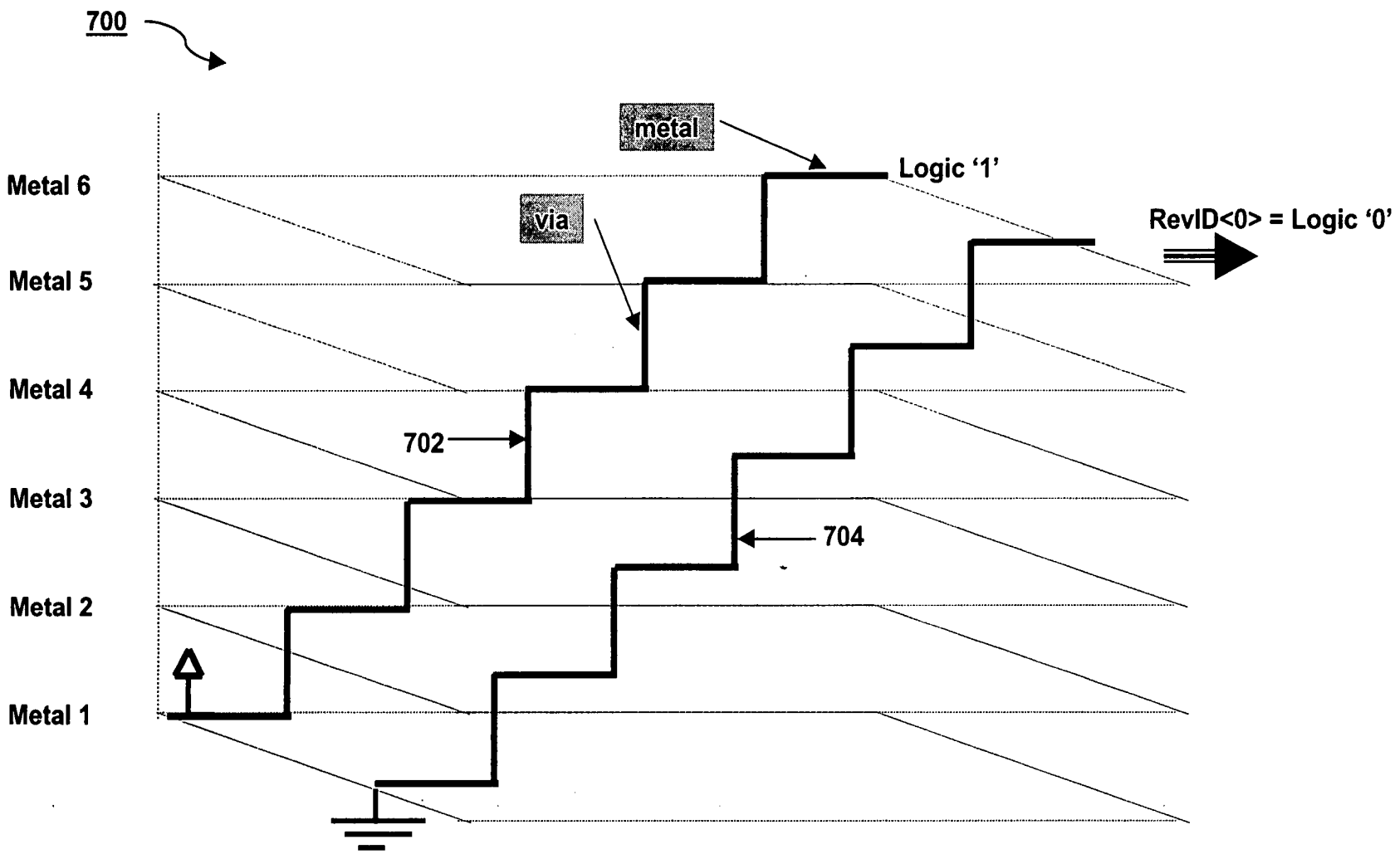

700
metal
Logic '1'
via
RevID<0> = Logic '0'
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
702
704

FIG. 7B

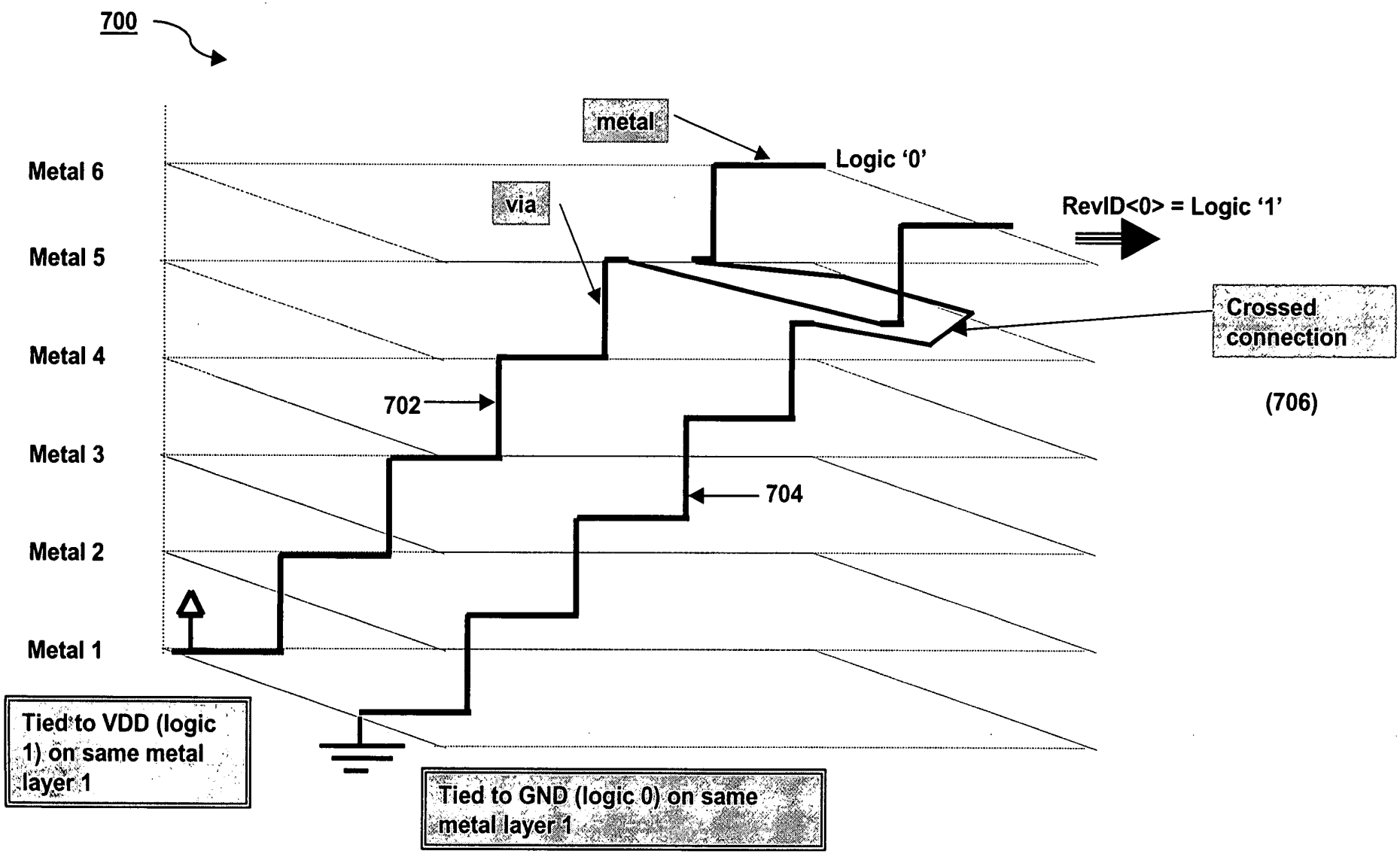

700
metal
Logic '0'
via
RevID<0> = Logic '1'
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Crossed connection
(706)
702
704
Tied to VDD (logic 1) on same metal layer 1
Tied to GND (logic 0) on same metal layer 1

FIG. 7C

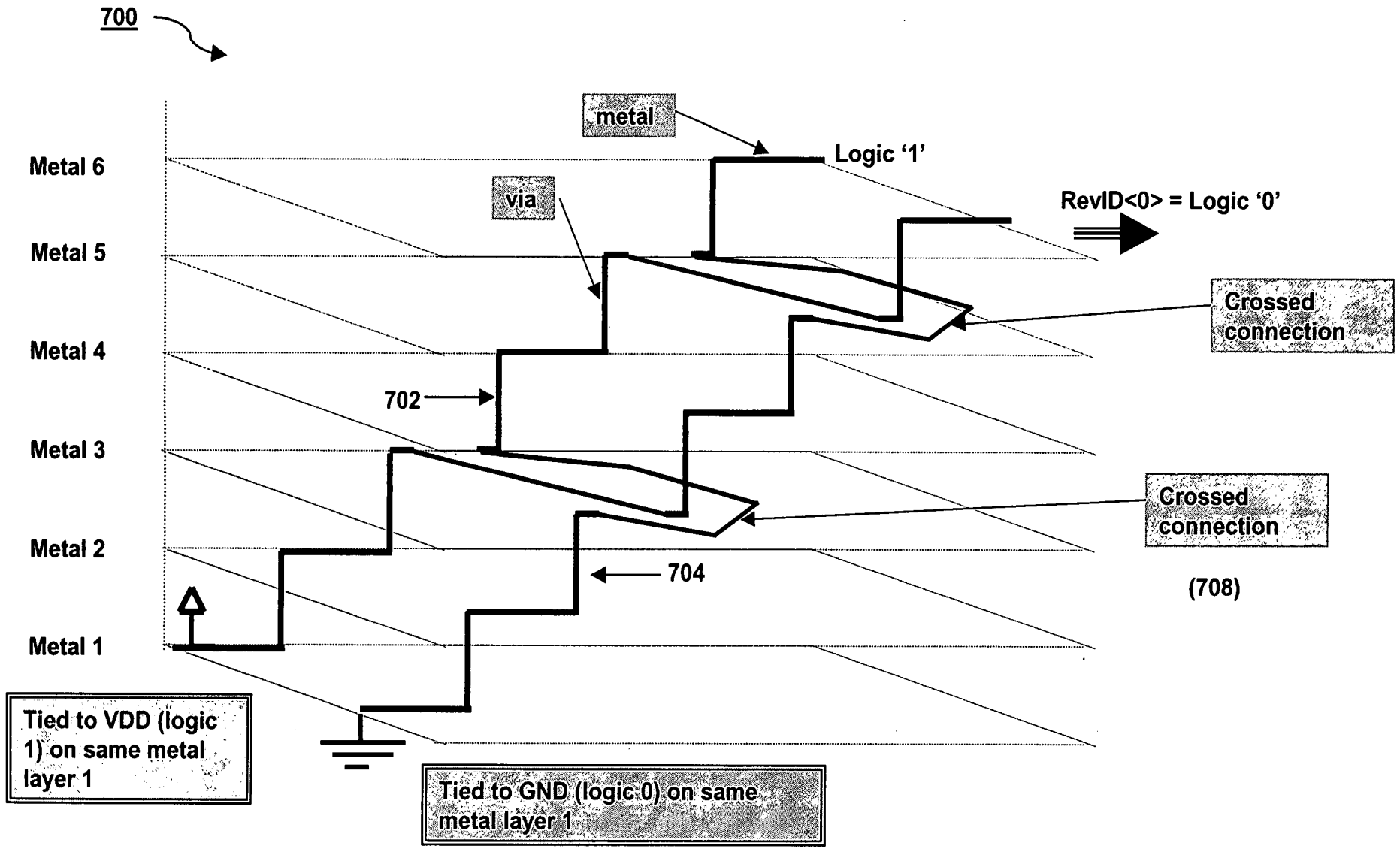

700
metal
Logic '1'
via
RevID<0> = Logic '0'
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Crossed connection
702
Crossed connection
704
(708)
Tied to VDD (logic 1) on same metal layer 1
Tied to GND (logic 0) on same metal layer 1

FIG. 7D

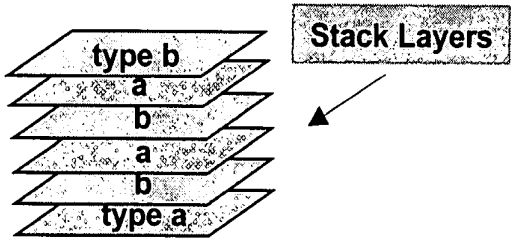

Stack Layers
type b
a
b
a
b
type a

FIG. 8A

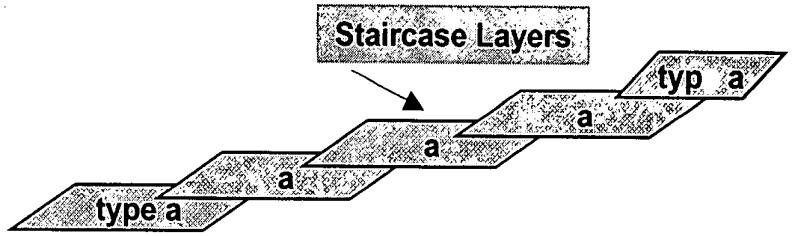

Staircase Layers
typ a
a
a
a
type a

FIG. 8B

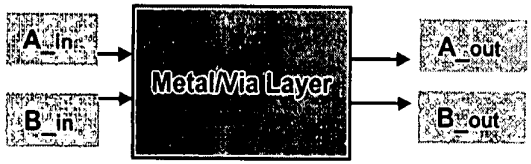

A_in
B_in
Metal/Via Layer
A_out
B_out

FIG. 9A

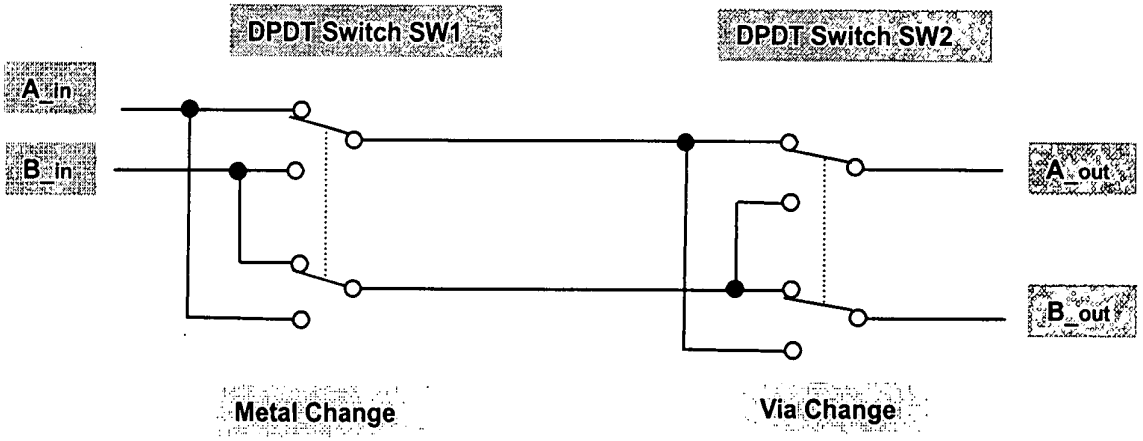

DPDT Switch SW1
DPDT Switch SW2
A_in
B_in
A_out
B_out
Metal Change
Via Change

FIG. 9B

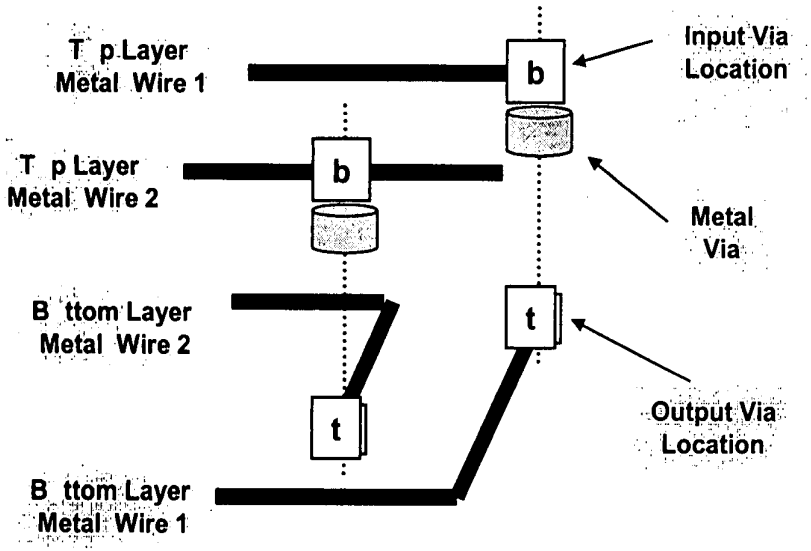
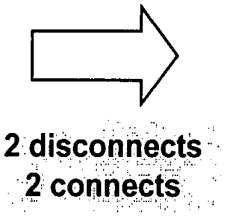

T p Layer
Metal Wire 1
T p Layer
Metal Wire 2
B ttom Layer
Metal Wire 2
B ttom Layer
Metal Wire 1
b
b
t
t
Input Via
Location
Metal
Via
Output Via
Location

FIG. 9C


2 disconnects
2 connects

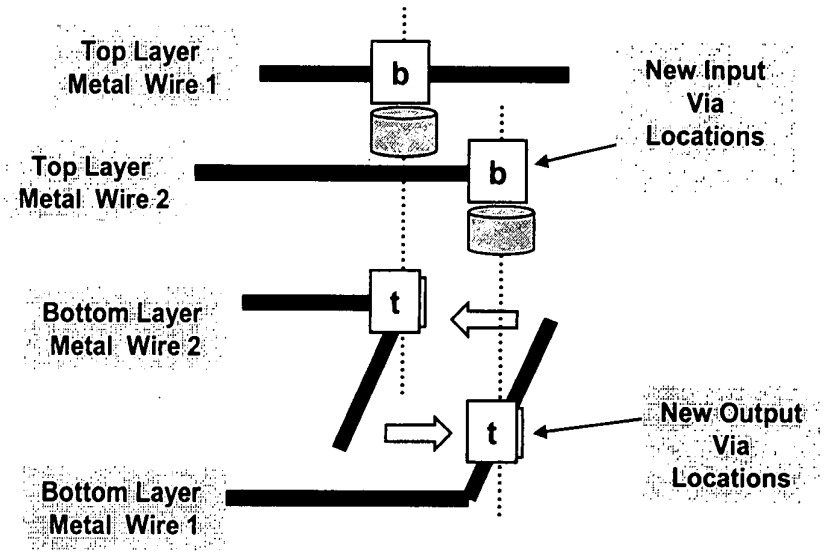

Top Layer
Metal Wire 1
Top Layer
Metal Wire 2
Bottom Layer
Metal Wire 2
Bottom Layer
Metal Wire 1
b
b
t
t
New Input
Via
Locations
New Output
Via
Locations

FIG. 9D

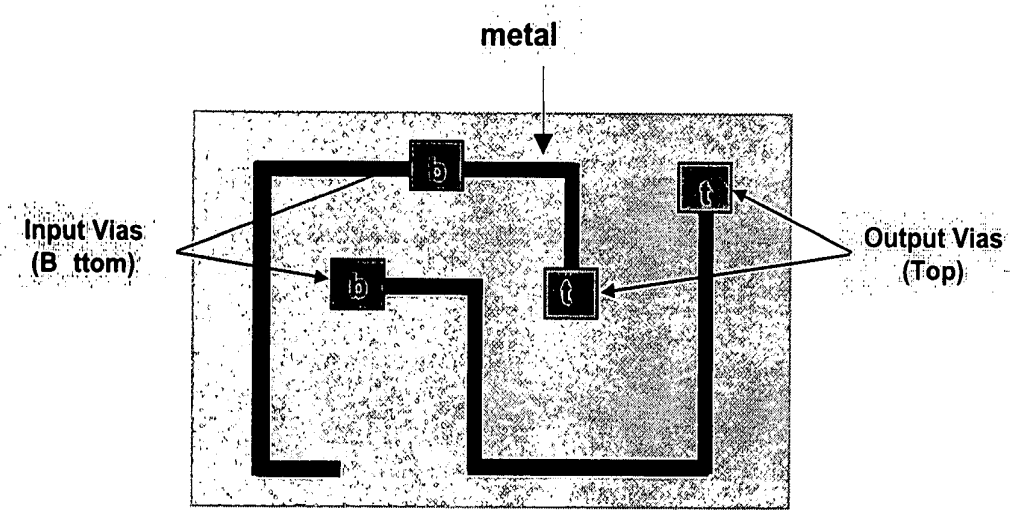


FIG. 10A

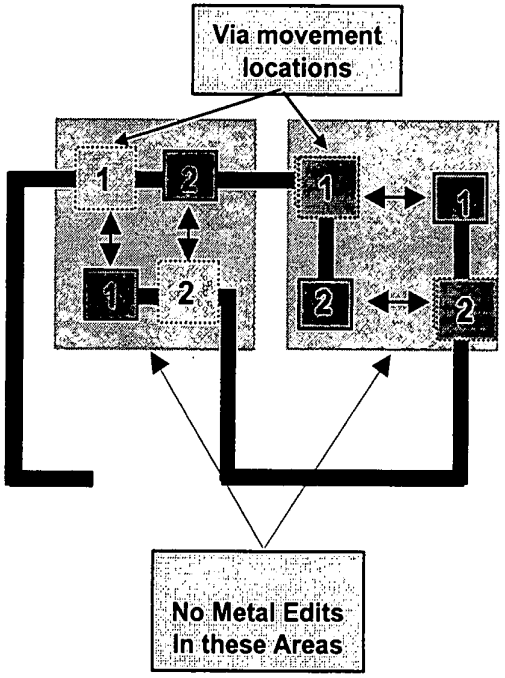
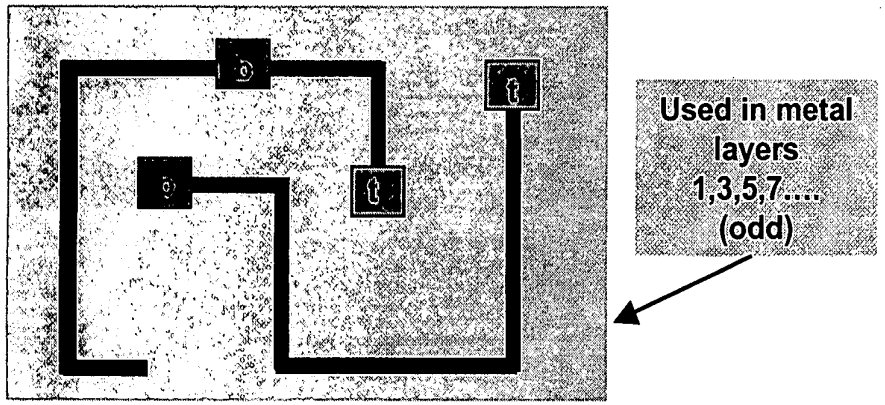
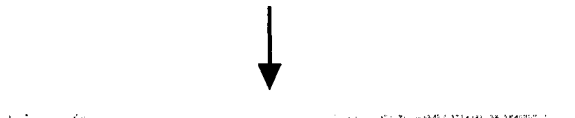


FIG. 10B

FIG. 11A



Basic Pattern



Basic Pattern w/ Metal Change (2 cuts, 2 jumps)

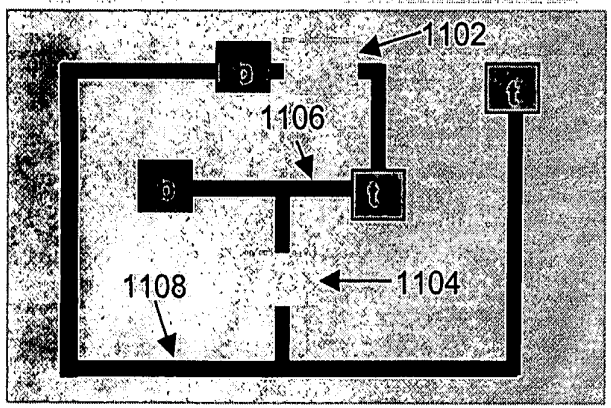
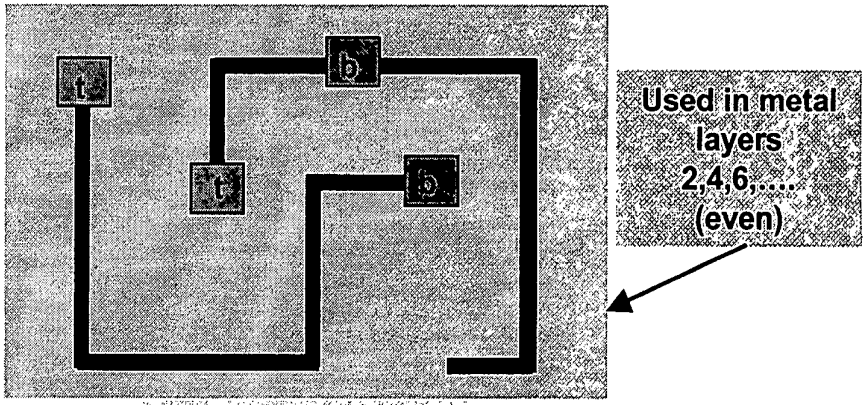


FIG. 11B

FIG. 11C



Flip Basic Pattern

Flip Basic Pattern w/ Metal Change (2 cuts, 2 jumps)

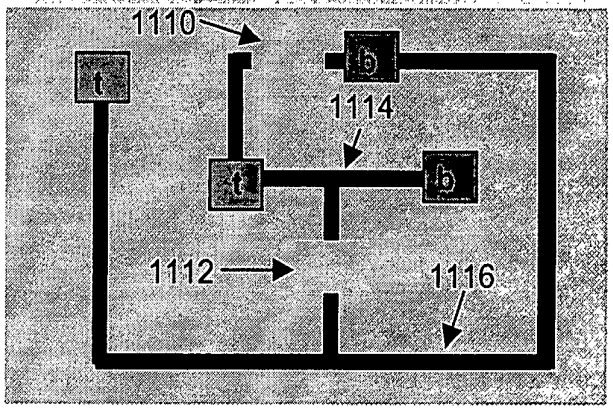
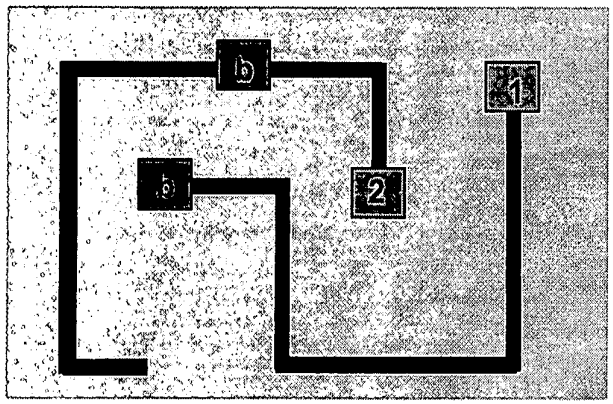


FIG. 11D

FIG. 12A



Basic Pattern

Basic Pattern w/ Via Change
(2 disconnects, 2 connects)

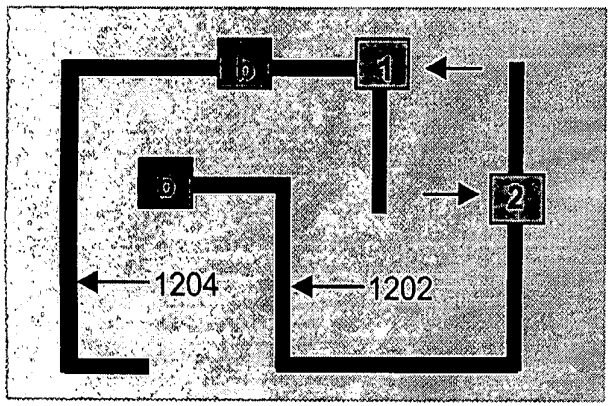
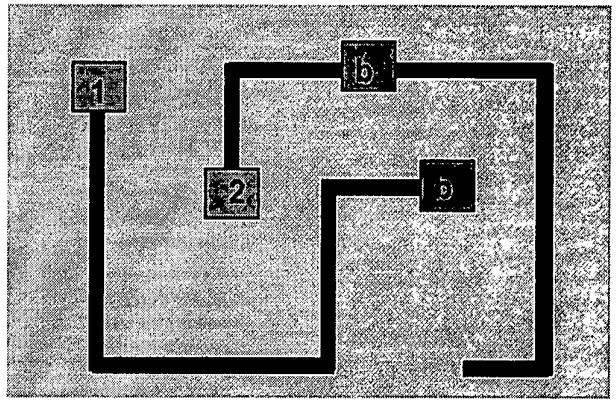


FIG. 12B

FIG. 12C



Flip Basic Pattern

Flip Basic Pattern w/ Via Change
(2 disconnects, 2 connects)

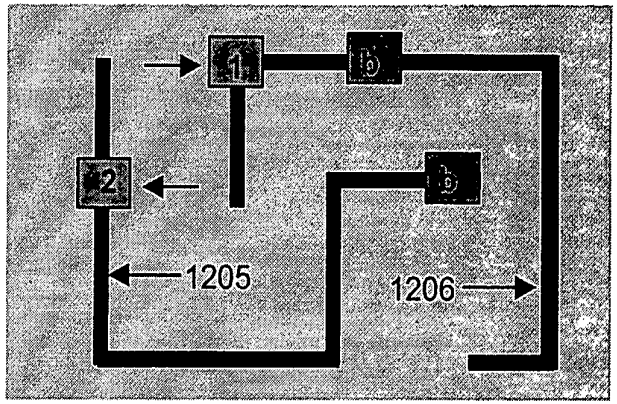


FIG. 12D

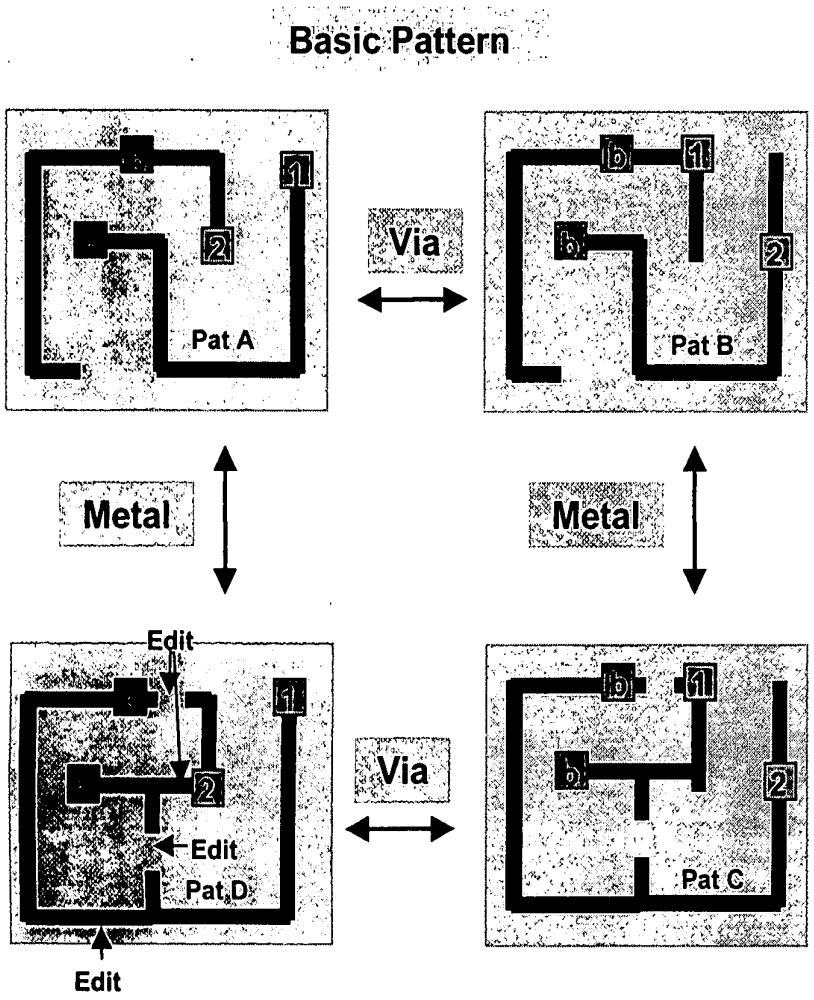

Basic Pattern
Pat A
Via
Pat B
Metal
Metal
Edit
Edit
Pat D
Via
Pat C
Edit

FIG. 13

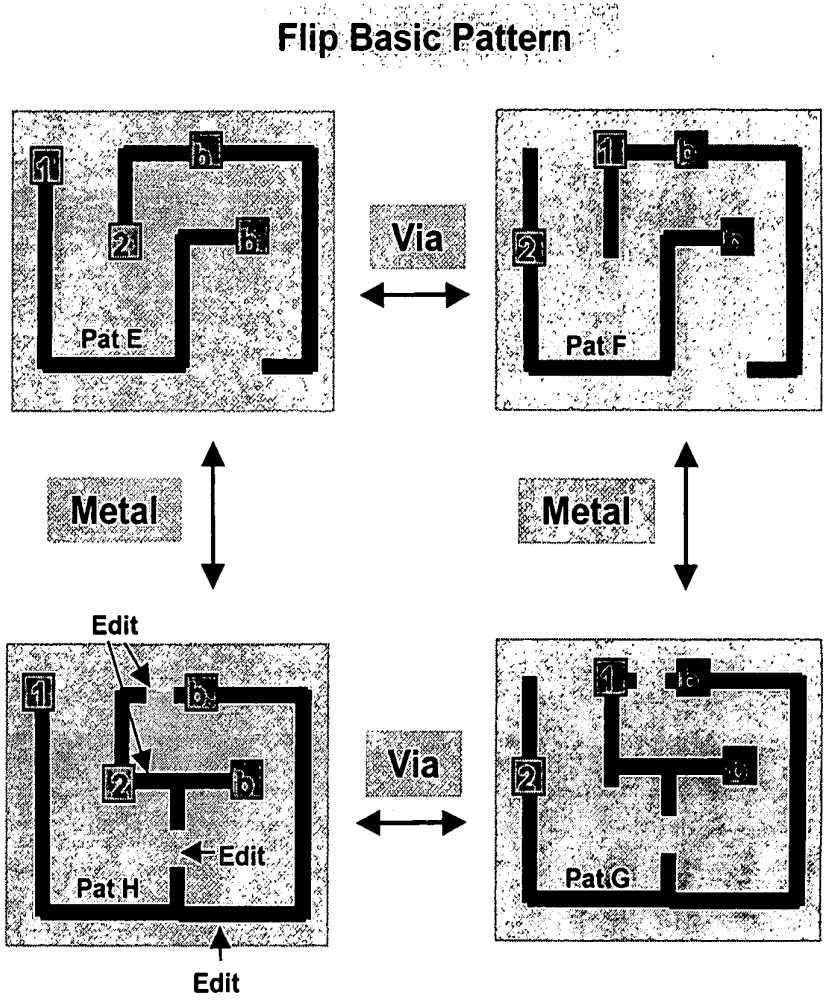

Flip Basic Pattern
Pat E
Via
Pat F
Metal
Metal
Edit
Pat H
Edit
Via
Pat G
Edit

FIG. 14

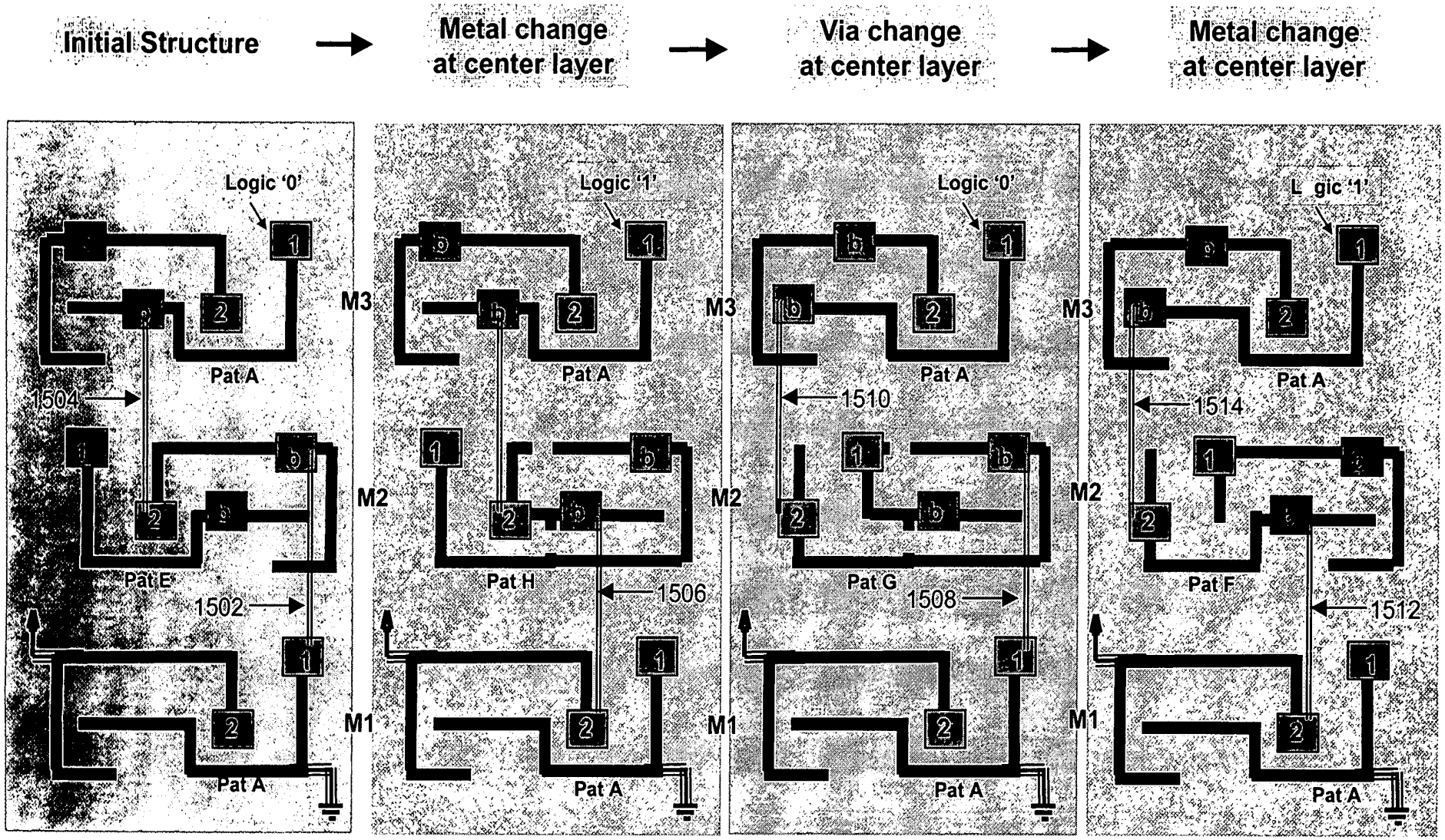


FIG. 15A FIG. 15B FIG. 15C FIG. 15D

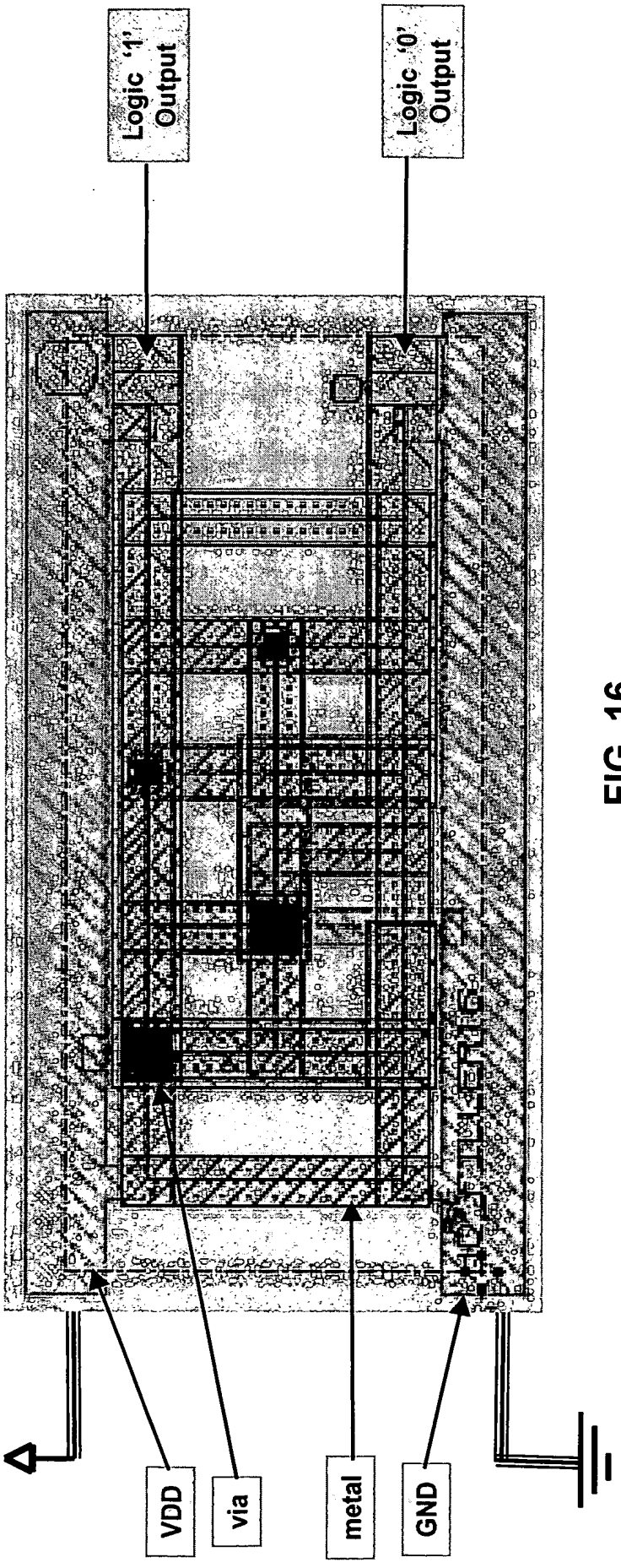


FIG. 16

FIG. 17A

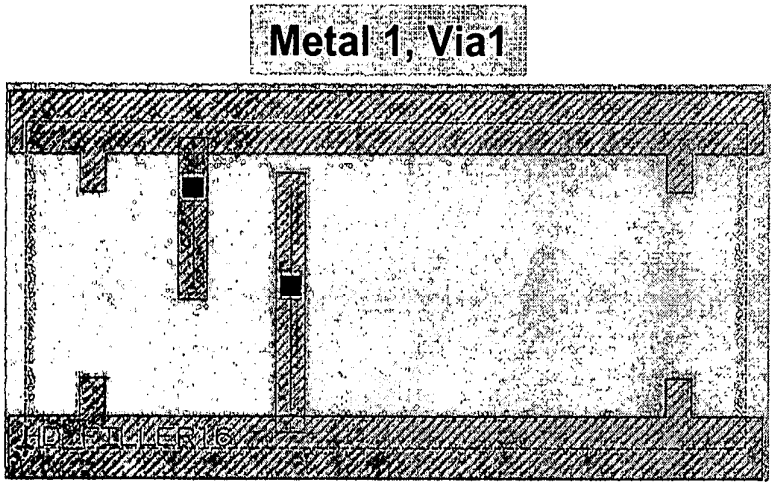
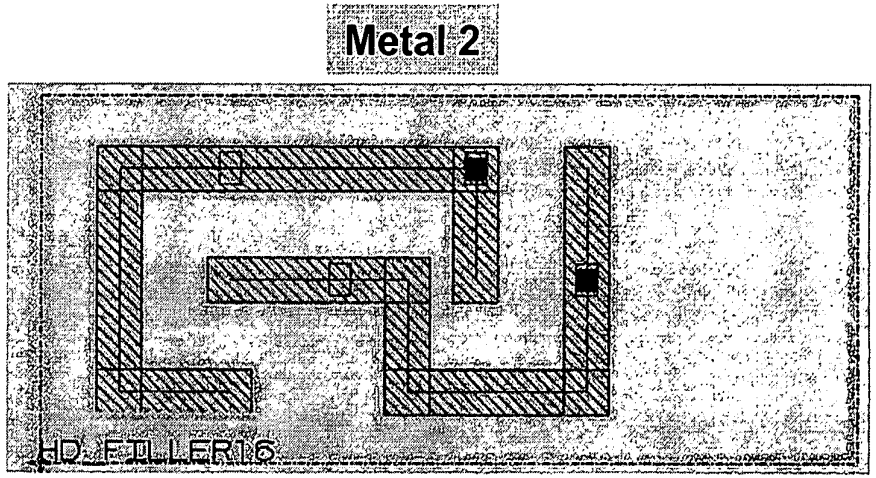


FIG. 17B



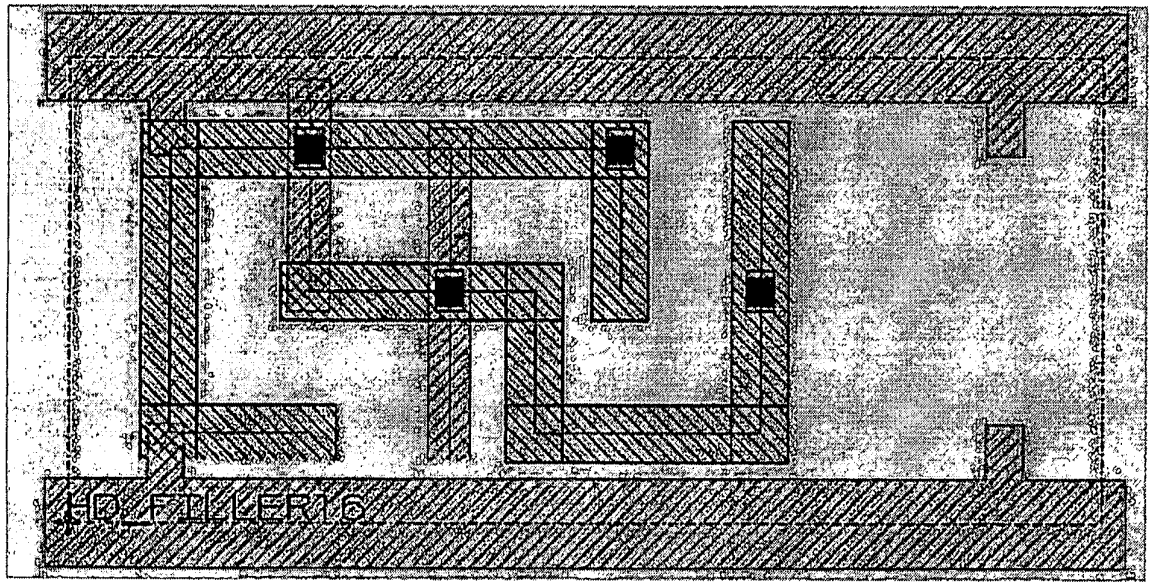
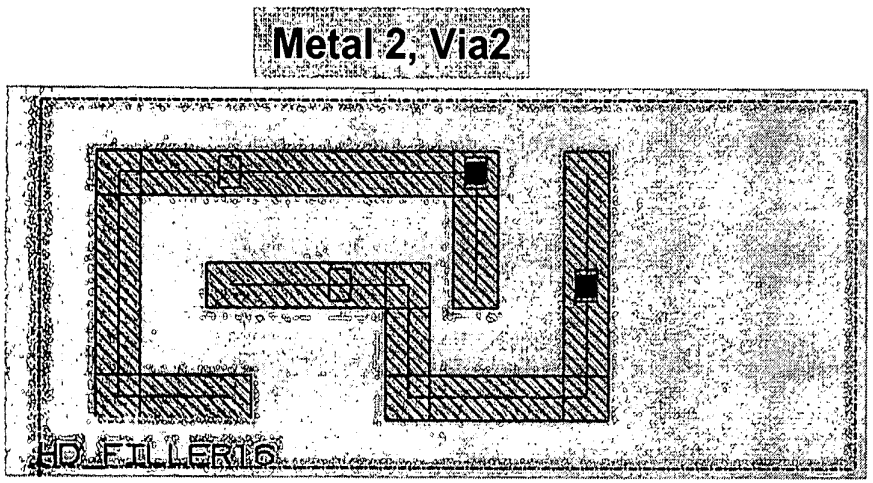
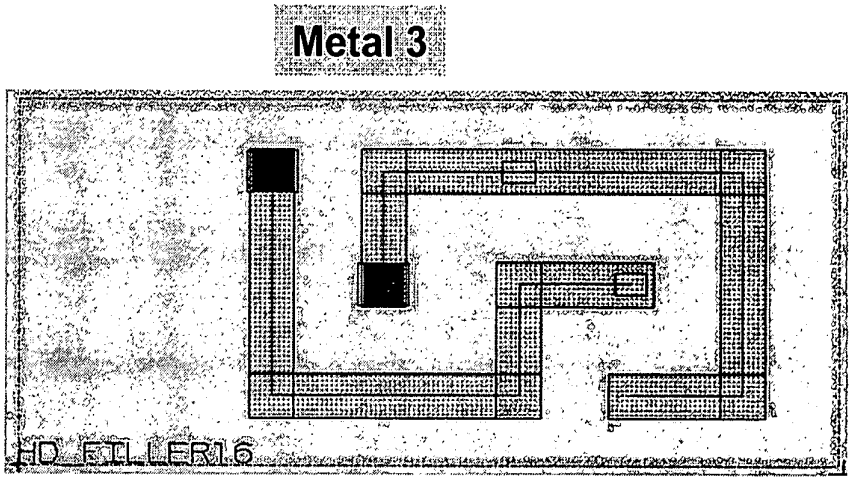


FIG. 17C

FIG. 18A

FIG. 18B





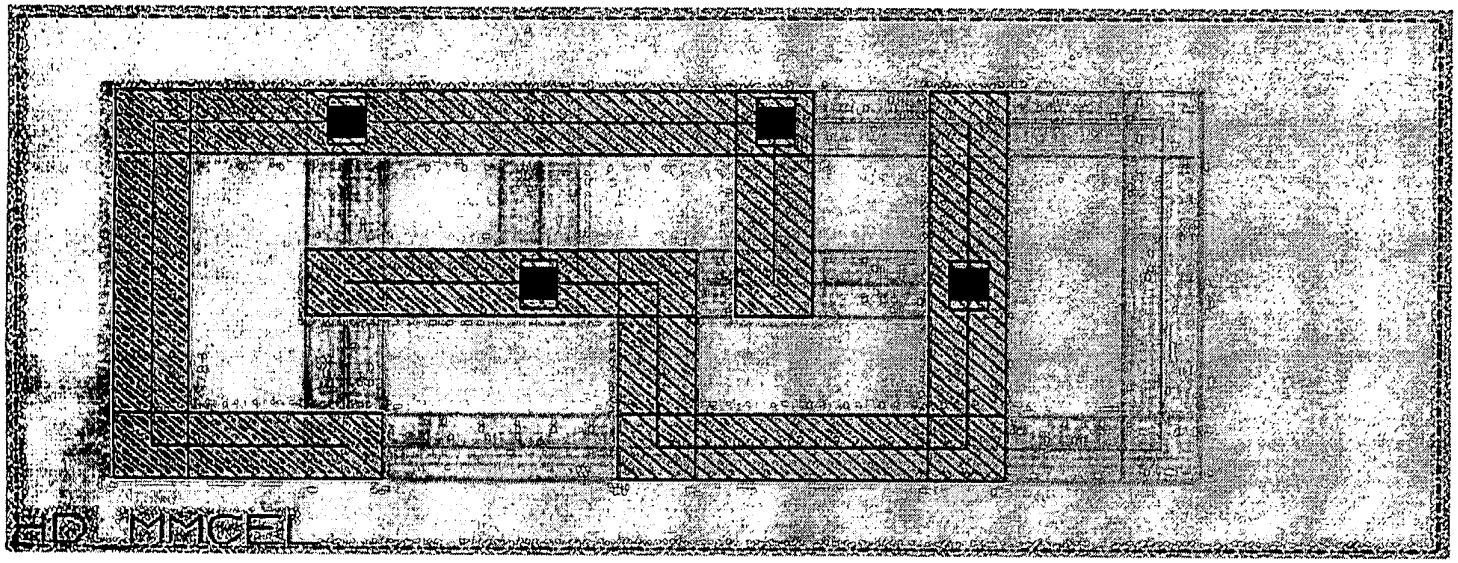


FIG. 18C

FIG. 19A

Metal 3, Via3

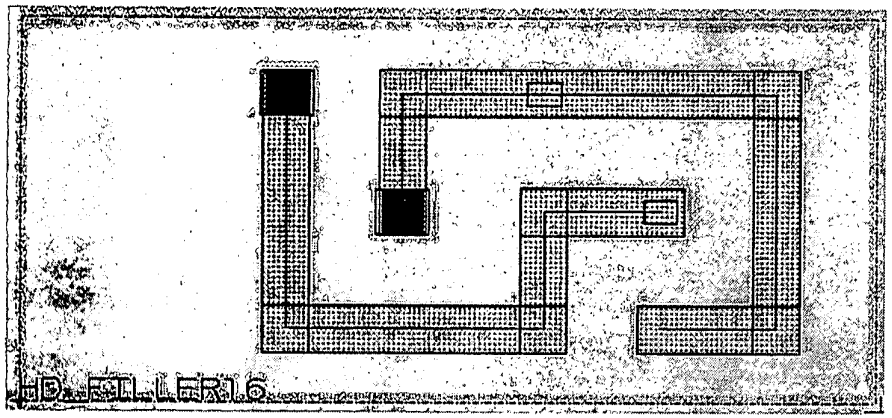
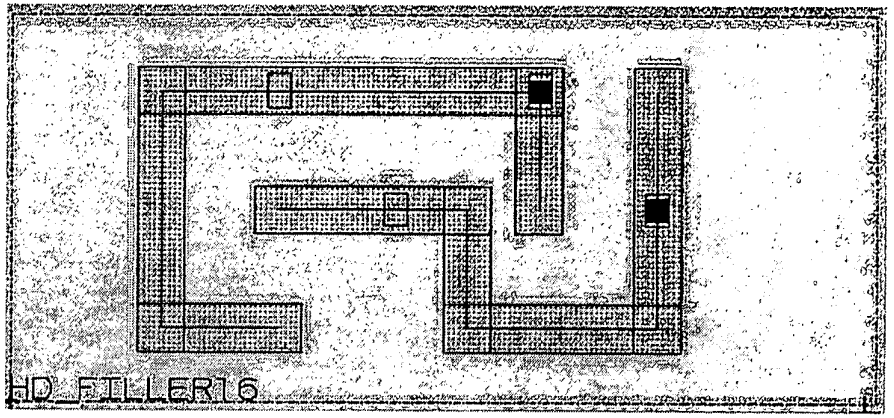
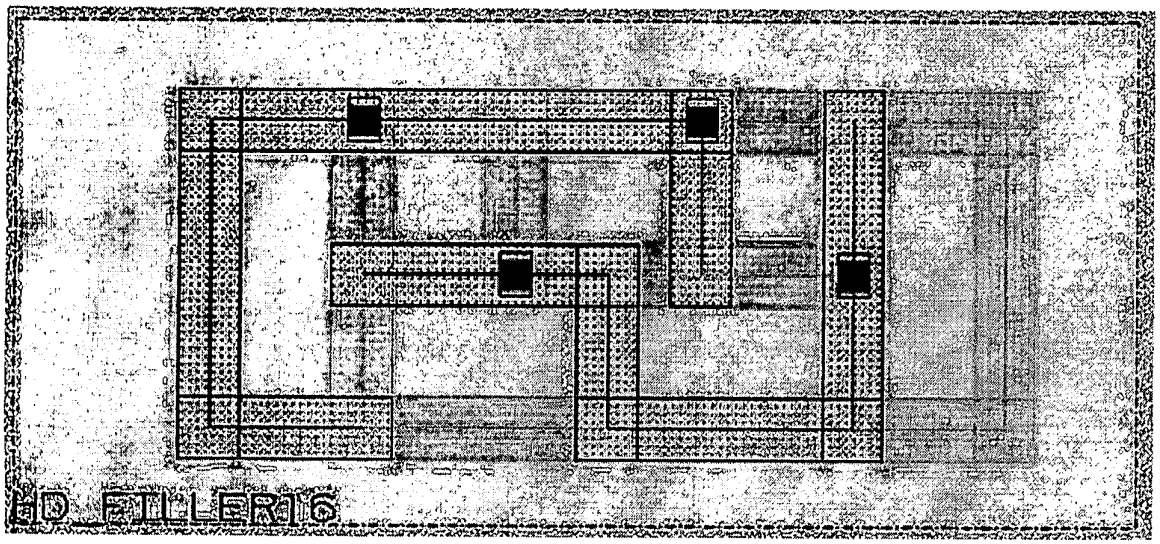


FIG. 19B

Metal 4





Metal 3, Via3,
Metal 4

FIG. 19C

FIG. 20A

Metal 4, Via4

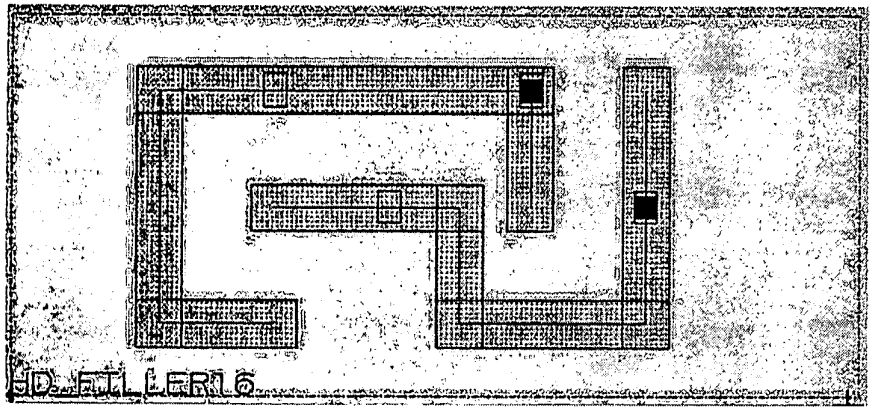
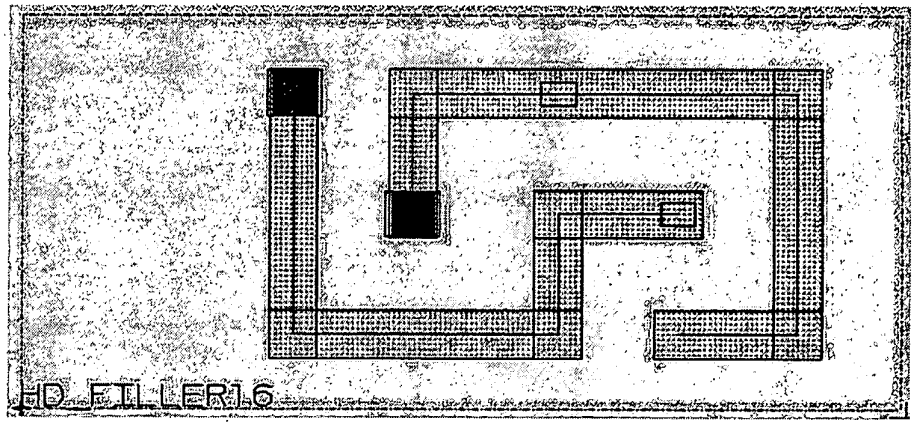
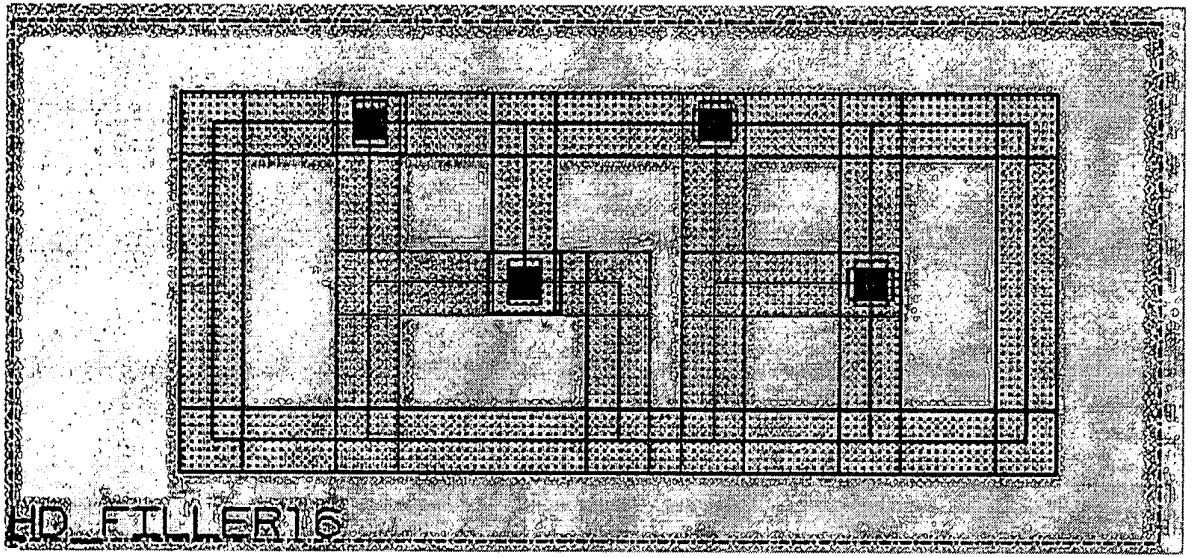


FIG. 20B

Metal 5





Metal 4, Via4, Metal 5

FIG. 20C

FIG. 21A

Metal 5, Via5

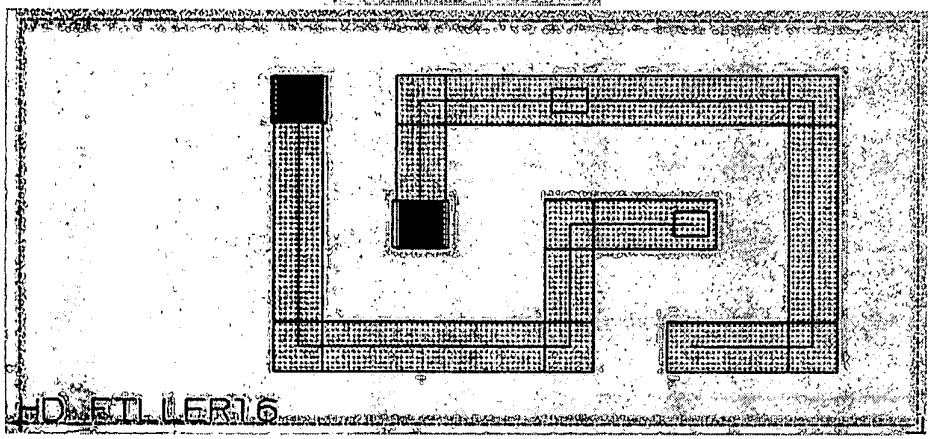
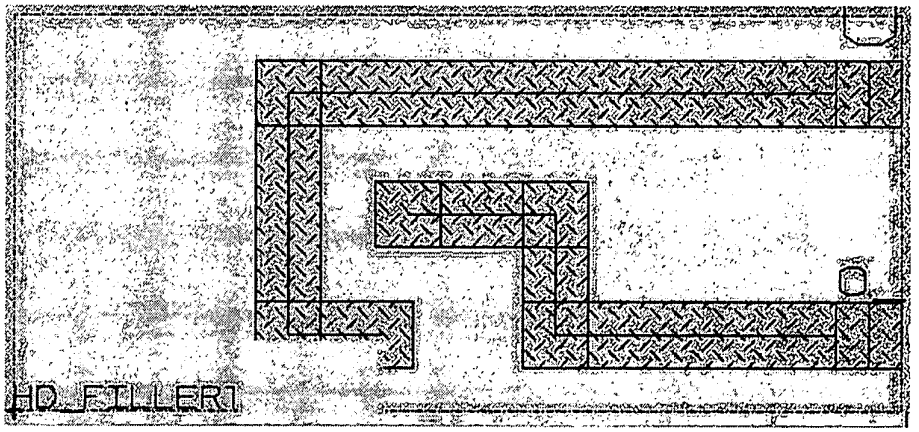
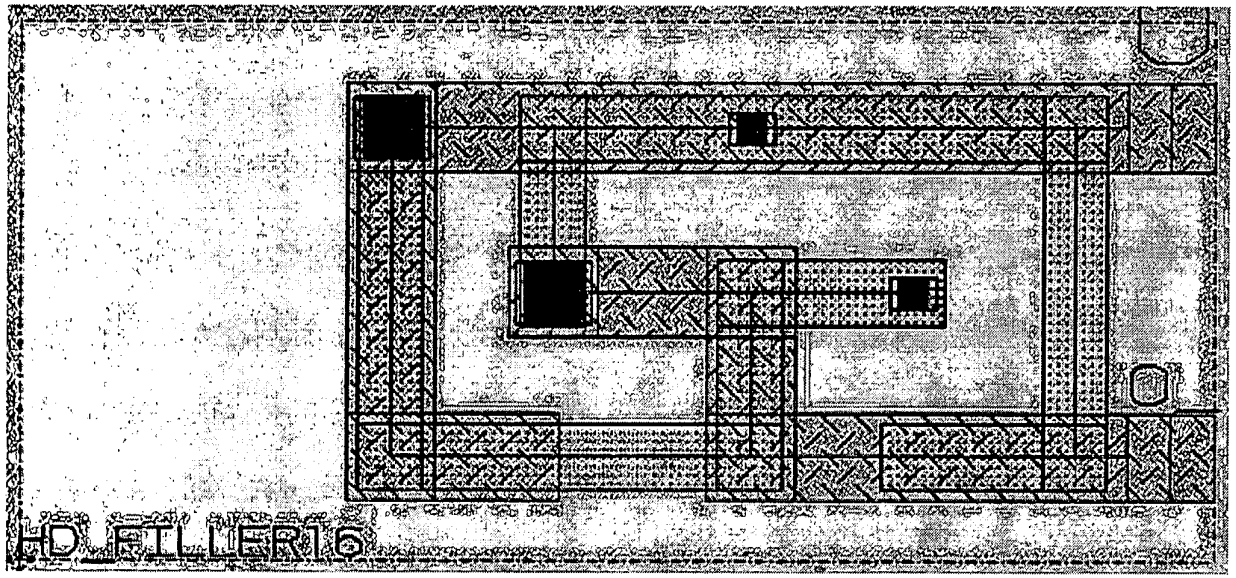


FIG. 21B

Metal 6





Metal 5, Via5, Metal 6

FIG. 21C

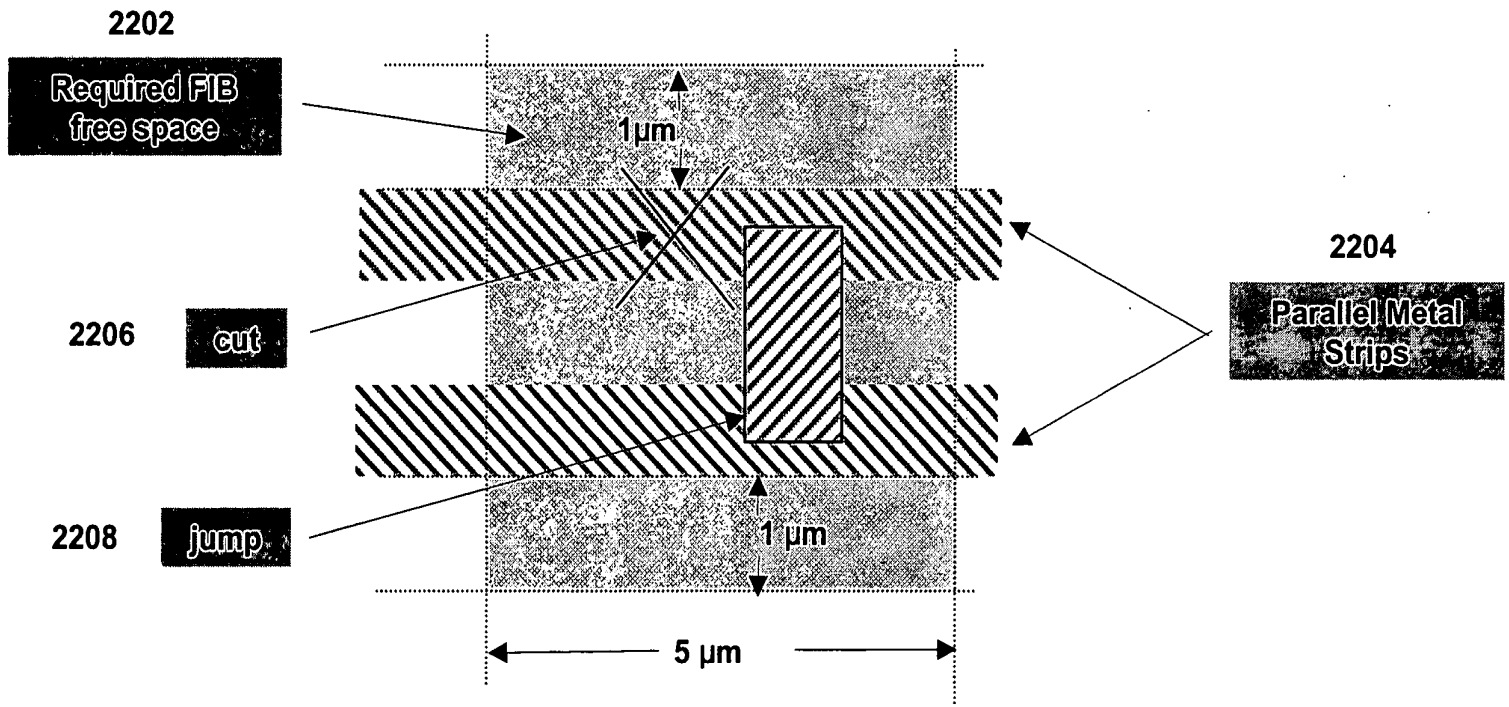

2202
Required FIB free space
1µm
2204
Parallel Metal Strips
2206
cut
2208
jump
1 µm
5 µm

FIG. 22

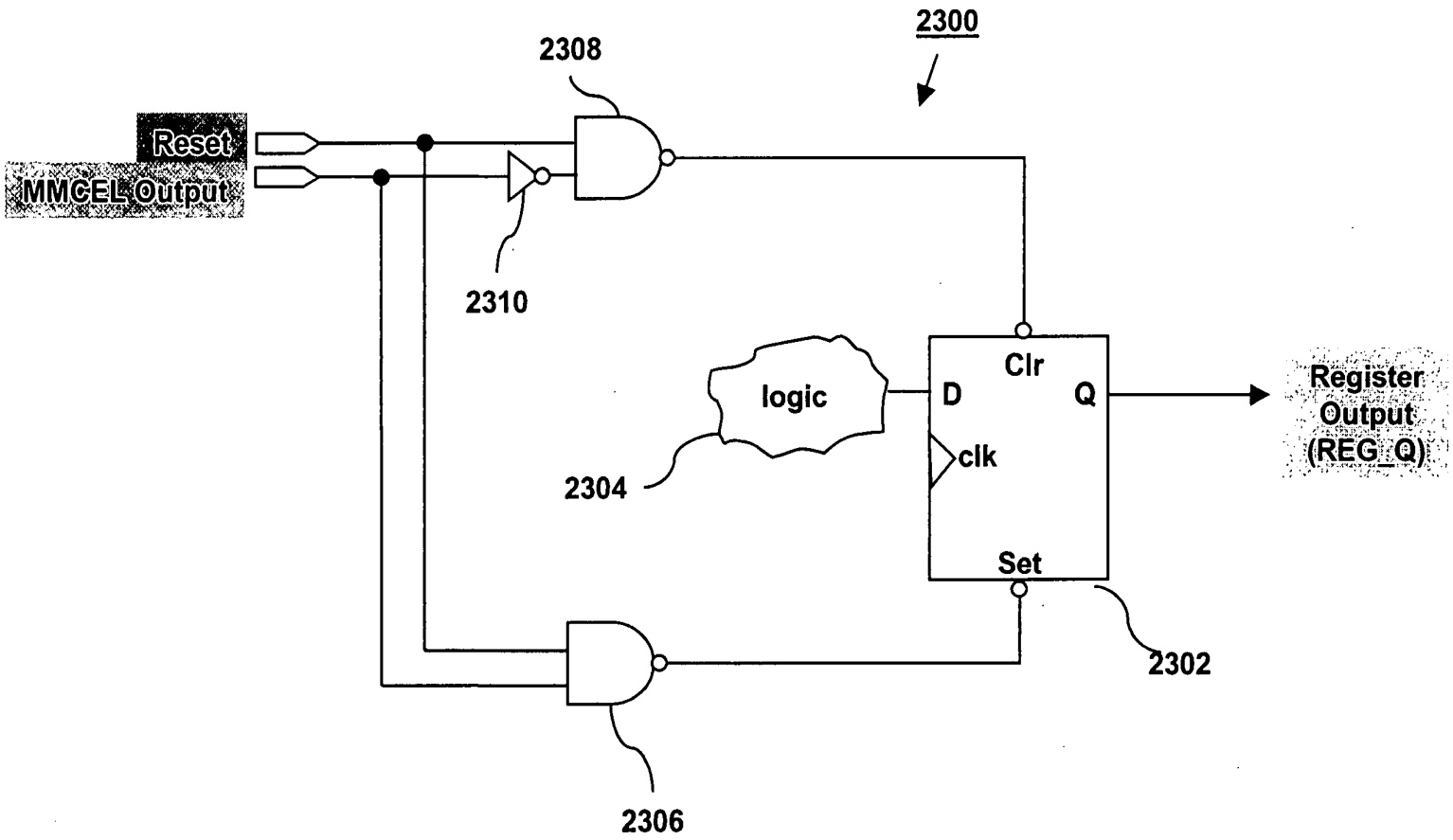

2300
2308
Reset
MMCEL Output
2310
logic
2304
Clr
D
Q
clk
Set
Register Output (REG_Q)
2302
2306

FIG. 23

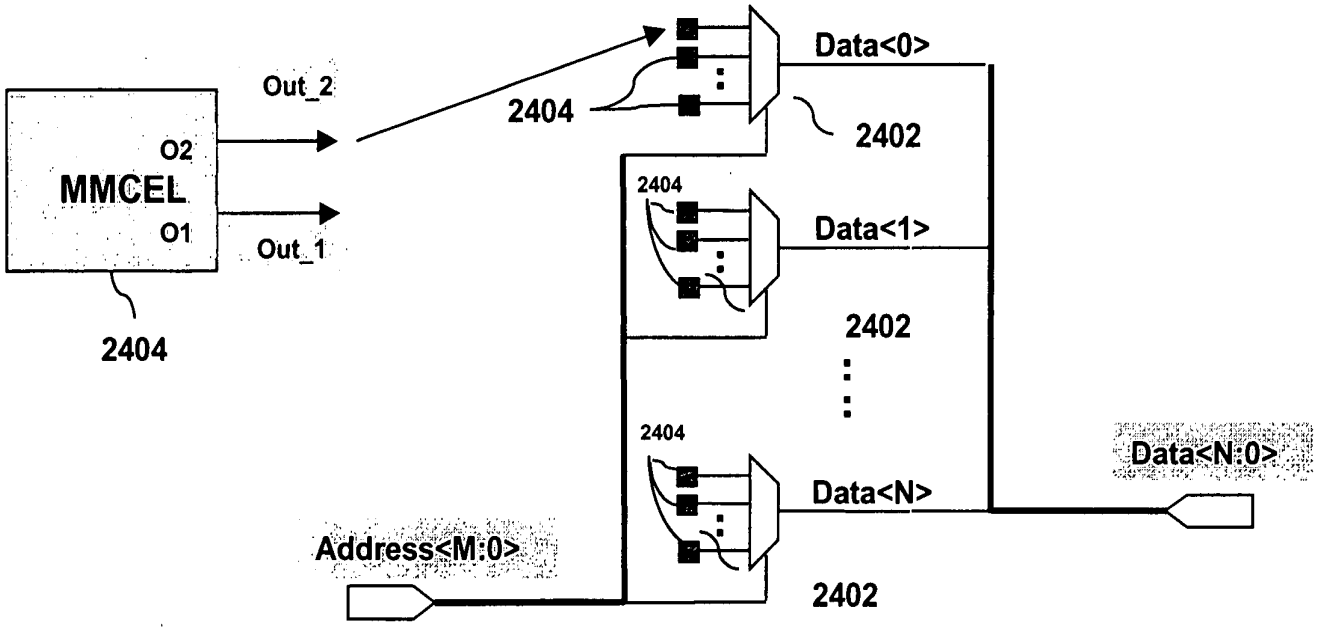

Out_2
O2
MMCEL
O1
Out_1
2404
2404
Data<0>
2402
2404
Data<1>
2402
2404
Data<N>
2402
Data<N:0>
Address<M:0>

FIG. 24